IN THE CLAIMS:

Kindly cancel claims 9 -16 without prejudice. Claims 1- 8 are in this application, as follows:

1. (Previously Presented) An early-late pulse accumulator comprising:

a first logic device configured to toggle a first output logic level upon receipt of an early pulse;

a second logic device configured to toggle a second output logic level upon receipt of a late pulse, wherein the first and second logic devices are configured to allow only one of the first and second output logic levels to be toggled at a time;

a first ripple divider configured to receive the first output logic level and to provide a scaled down count of the number of times the first logic device toggles;

a second ripple divider configured to receive the second output logic level and to provide a scaled down count of the number of times the second logic device toggles;

a first synchronizing logic device configured to receive the scaled down count of the number of times the first logic device toggles and to generate a first terminal count signal proportional to the number of early pulses received by the first logic device;

a second synchronizing logic device configured to receive the scaled down count of the number of times the second logic device toggles and to generate a second terminal count signal proportional to the number of late pulses received by the second logic device; and

an integrator configured to receive the first and second terminal count signals and generate a net early-late count.

2. (Original) The accumulator of claim 1 wherein the integrator is configured to increment upon receipt of the first terminal count signals and decrement upon receipt of late terminal count signals.

3. (Original) The accumulator of claim 1 wherein the first logic device comprises a first XOR gate configured to toggle a first flip-flop, and wherein the second logic device comprises a second XOR gate configured to toggle a second flip-flop.

4. (Original) The accumulator of claim 1 wherein the first logic device and the second logic device are configured to toggle as clocked by a transition in the data signal.

5. (Original) The accumulator of claim 4 wherein the transition in the data signal is a rising data signal.

6. (Original) The accumulator of claim 4 wherein the transition in the data signal is a falling data signal.

7. (Original) The accumulator of claim 4 wherein the transition in the data signal comprises an alternating rising data signal and falling data signal.

8. (Previously presented) A pulse accumulator comprising:

a logic device for receiving more than one early pulse and more than one late pulse;

an early ripple divider configured to count the early pulses on a scaled down basis;

a late ripple divider configured to count the late pulses on a scaled down basis;

an early pulse synchronizing device configured to receive the scaled down early pulses and to generate an early terminal count corresponding to the number of early pulses;

a late pulse synchronizing device configured to receive the scaled down late pulses and to generate a late terminal count corresponding to the number of late pulses;

an integrator configured to receive a scaled down clock signal and to increment upon receipt of the early terminal count signals and decrement upon receipt of the late terminal count signals.

9 - 16 (Canceled)